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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/466,405	12/17/1999	FARRELL L. OSTLER	PHA23.891	1131

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EXAMINER
MEONSKE, TONIA L

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/466,405	Applicant(s) OSTLER ET AL.	
	Examiner Tonia L Meonske	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 December 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Papers Submitted

1.) It is hereby acknowledged that the following papers have been received and placed of record in the file: Information Disclosure Statement on March 19, 2001, Change of Address/Power of Attorney on February 7, 2000, and Declaration and Fees on December 27, 1999.

Drawings

2.) The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: 245 on page 11, line 6 and 10. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3.) The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 100, C_j, C_k, C_m, R_a, R_b, 273, and 284. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4.) The drawings are objected to because in Figure 1, it's not clear how the selectors (141-149) are duplicated as indicated by the ellipses. The selectors all appear to be selecting different things, so it is unclear how the selectors can be duplicated when they are different.

Specification

5.) The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

6.) The Abstract is object to for containing over 150 words.

7.) Applicant is reminded of the proper language and format for an abstract of the disclosure.

8.) The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

9.) The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

10.) The disclosure is objected to because of the following informalities: On page 9, lines 11-13 the blanks need to be filled in, on page 2, line 1, please change "As" to "In". In addition, on page 11, lines 17-19, format 208 does indeed have a corresponding Jump field, but on lines 18-19 it states that format 208 is "without a corresponding Jump field." The examiner believes that format 208 should be changed to 206.
(a) Appropriate correction is required.

Claim Rejections - 35 USC § 102

11.) The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12.) Claims 1-9 are rejected under 35 U.S.C. 102(b) as being clearly anticiapted by Cocke et al., US Patent 3,577,189.

13.) Referring to claim 1, Cocke et al. have taught a processor that is configured to execute program instructions that are stored in a memory, comprising a default-register that is configured to contain a default destination-address, and wherein the program instructions include: a first instruction that is configured to cause the processor to load a specific address into the default-register to form the default-destination-address (Column 1, line 73-column 2, line 28, the effective branch address is calculated in an instruction to be used for a subsequent exit instruction, so the effective branch address must inherently be stored in a default-register in order to be used in a subsequent instruction), and a second instruction that is configured to cause the processor to subsequently execute program instructions that are located in the memory at the default-destination-address contained in the default-register (Column 1, line 73-column 2, line 28, exit instruction).

14.) Referring to claim 2, Cocke et al. have taught the processor of claim 1, as described above, wherein the second instruction includes a condition test and is further configured to cause the processor to execute program instructions that are located at the default-destination-address in dependence upon a result of the condition test. (Column 1, line 73-column 2, line 28, there is an instruction that tests and determines whether on not the branch is to be taken)

15.) Referring to claim 3, Cocke et al. have taught the processor of claim 1, as described above, wherein the default-register is further configured to contain a default-condition-test, and wherein the second instruction is further configured to cause the processor to execute program instructions that are located at the default-destination-address in dependence upon a result of the default-condition-test contained in the default-register.

(Column 1, line 73-column 2, line 28, there is an instruction that tests and determines whether on not the branch is to be taken, the result of the condition test is saved in a default register, the exit instruction depends on the condition test result saved in the default register)

16.) Referring to claim 4, Cocke et al. have taught the processor of claim 1, as described above, wherein the second instruction is further configured to cause the processor to execute program instructions that are located at the default-destination-address in dependence upon a result of a prior condition-test. (Column 1, line 73-column 2, line 28, there is an instruction that tests and determines whether on not the branch is to be taken at the effective branch, or default-destination address, in a subsequent exit instruction)

17.) Referring to claim 5, Cocke et al. have taught the processor of claim 1, as described above, wherein the default-register is further configured to contain a default-condition-test, and wherein the program instructions further include: a third instruction that is configured to cause the processor to execute program instructions that are located at another specified address in dependence upon a result of the default-condition-test contained in the default-register. (Column 1, line 73-column 2, line 28, there is an instruction that tests and determines whether on not the branch, or second instruction, is to be taken, the result of the condition test is saved in a default register, the exit instruction depends on the condition test result saved in the default register, the exit branches to the effective branch address if it is determined that the branch is to be taken, and the next subsequent instruction is executed if the branch is not taken)

18.) Referring to claim 6, Cocke et al. have taught a processor that is configured to execute program instructions that are stored in a memory, comprising a default-register that is configured to contain a default condition-test and wherein the program instructions include: a first instruction that is configured to cause the processor to load a specified condition into the default-register to form the default-condition-test (Column 1, line 73-column 2, line 28, there is an instruction that determines whether the branch is to be taken or not, this value is inherently stored in a default-register), and a second instruction that is configured to cause the processor to subsequently execute program instructions that are located in the memory at a destination-address, based on a result of the default-condition-test. (Column 1, line 73-column 2, line 28, there is an instruction that tests and determines whether on not the branch, is to be taken, the result of the condition test is saved in a default register, the exit instruction depends on the condition test result of the default-condition-test saved in the default register)

19.) Referring to claim 7, Cocke et al. have taught a method of controlling a sequence of program instructions comprising: executing a first instruction that specifies a destination address (Column 1, line 73-column 2, line 28, there is an instruction that specifies the effective branch address), executing a second instruction that causes thedestination address to become a next instruction address (Column 1, line 73-column 2, line 28, exit instruction), and executing a third instruction that is located at the next instruction address. (Column 1, line 73-column 2, line 28, instructions beginning at the effective branch address are transmitted to the storage system and the instructions are executed starting with the instruction located at the effective branch address)

20.) Referring to claim 8, Cocke et al. have taught the method of claim 7, as described above, further including executing a fourth instruction, before executing the second instruction, that specifies a condition-test, and wherein causing the destination-address to become the next instruction address is dependent upon a result of the condition-test when the second instruction is executed. (Column 1, line 73-column 2, line 28, it is determined in a fourth whether the branch is to be taken or not, if the branch is taken then the next instruction address is the effective branch address, if the branch is not to be taken the next instruction address is the next address)

21.) Referring to claim 9, Cocke et al. have taught the method of claim 7, as described above, further including saving a result of a condition-test, before executing the second instruction (Column 1, line 73-column 2, line 28, it is determined whether or not the branch is to be taken prior to the exit instruction, and the result in inherently saved), and wherein causing the destination-address to become the next instruction address when executing the second instruction is dependent upon the result of the condition-test. (Column 1, line 73-column 2, line 28, there is an instruction that tests and determines whether on not the branch, or second instruction, is to be taken, the result of the condition test is saved, the exit instruction depends on the saved condition test result, the exit branches to the effective branch address if it is determined that the branch is to be taken, and the next subsequent instruction is executed if the branch is not taken)

Conclusion

22.) The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a

rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

(a) Schlansker et al, US Patent 5,664,135, have taught an apparatus and method for reducing delays due to branches..

(b) Sturges et al., US Patent 5, 961, 637, have taught a split branch system utilizing separate set branch, condition and branch instruction and including dual instruction fetchers.

23.) Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 8-4:30.

24.) If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

25.) Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

tlm
August 12, 2002

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100